3. The package of claim 1, wherein the plurality of electrical connections between the die bond pads and the package bond pads are made by TAB.

4. The package of claim 1, wherein the plurality of electrical connections between the die bond pads and the package bond pads are made by solder balls.

5. The package of claim 1, wherein the printed wiring board has a metal core, one or more build-up layers and a solder mask passivation layer, where each buildup layer comprises an organic dielectric layer with vias and a patterned metal layer.

6. The package of claim 5, wherein the circuitry of the printed wiring board is on one side, and the printed wiring board does not contain through vias or plated through holes (PTHs).

7. The package of claim 5, wherein the metal core is made from a material which has a TCE to match an electronic board on which the semiconductor package is mounted.

8. The package of claim 7, wherein the material is copper, copper alloy, aluminum, or alloy of aluminum.

9. The package of claim 5, wherein the metal core is made from a material with a TCE to match the integrated circuit die.

10. The package of claim 9, wherein the material is CuW, Mo, CuMo, copper clad Mo, Invar, and copper clad Invar.

11. The package of claim 5, wherein the metal core is made from a material with a TCE half way between the integrated circuit die and the electronic board on which the semiconductor package is mounted.

12. The package of claim 11, wherein the material is stainless steel.

13. The package of claim 1, wherein the plurality of package pads are arranged in an array, where the array need not be fully populated with package pads and particularly the center of the array is not populated with package pads.

14. The package of claim 13, wherein the pitch of the array, the distance from the center of one package pad to the center of an adjacent populated package pad is 0.5mm, 0.65mm, 0.8mm, 1.0mm and 1.27mm.

15. The package of claim 13, wherein there are a plurality of package solder balls attached to respective selected package pads.

16. The package of claim 13, wherein there are a plurality of package pins attached to respective selected package pads.

17. The package of claim 1, wherein the plurality of package pads are arranged in a row along the periphery of the printed wiring board.